2002 High Density Microelectronics Roadmap for Space Applications

Lissa Galbraith, PhD
Mail Stop 125-152, National Aeronautics and Space Administration, California Institute of Technology Jet Propulsion Laboratory, 4800 Oak Grove Drive, Pasadena, California, 91109-8099 USA

This Roadmap for high density interconnect microelectronics introduces current technologies in use, related strategic issues, and research recommendations for space applications. The American Optoelectronics Industry Development Association forecasts that voice will occupy only one per cent of network traffic by 2005. Chip computational power is expected to reach 9,800 MIPS by 2005. The average number of I/O interconnects per chip is expected to reach 2,500 by 2002. The smallest package feature size is anticipated to be 0.1 micrometers or less by 2005. The number of transistors in successive Intel microprocessors has evolved from 6,000 with the advent of the Pentium in 1995 to an expected 30,000 by the end of 2000. Satisfying these demands will require enhanced electronic performance with an associated improvement in packaging performance and better relief from thermal and mechanical stresses.

The traditional hierarchical network topology of circuit switching will need to evolve to a flat network topology for packet switching which is more conducive to data and Internet traffic. Technology development required to support this includes single tunable lasers to replace multiple fixed wavelength lasers, ultrawide bandwidth fibers and optical amplifiers, and large capacity optical cross connects and routers for handling multi-terabit information rates on a single fiber. Also needed is the development of 13 GHz laser drivers and amplifiers, evolving 10Gb/s to be as affordable as 2.5Gb/s in general, defining standard interfaces for 10Gb/s metallic or fiber, as well as further development of receivers and transmitters to use wave division multiplexing for 10Gb/s traffic.

Technical challenges and directions for high density interconnect microelectronics packaging are discussed. Forecasts and recommendations for research direction are given for components, materials, and packaging.